METHOD AND SYSTEM FOR ADJUSTING THE TIMING OFFSET BETWEEN A CLOCK SIGNAL AND RESPECTIVE DIGITAL SIGNALS TRANSMITTED ALONG WITH THAT CLOCK SIGNAL, AND MEMORY DEVICE AND COMPUTER SYSTEM USING SAME

ABSTRACT OF THE DISCLOSURE

A method and circuit adaptively adjust respective timing offsets of digital signals relative to a clock output along with the digital signals to enable a latch receiving the digital signals to store the signals responsive to the clock. A phase command for each digital signal is stored in an associated storage circuit and defines a timing offset between the corresponding digital signal and the clock. The clock is output along with each digital signal having the timing offset defined by the corresponding phase command and the digital signals are captured responsive to the clock and evaluated to determine if each digital signal was successfully captured. A phase adjustment command adjusts the value of each phase command. These operations are repeated for a plurality of phase adjustment commands until respective final phase commands allowing all digital signals to be successfully captured is determined and stored in the storage circuits.